DDR SDRAM, The Next PC Mainstream DRAM Technology

Platform 2001 Presentation

January 2001

Hyundai Electronics

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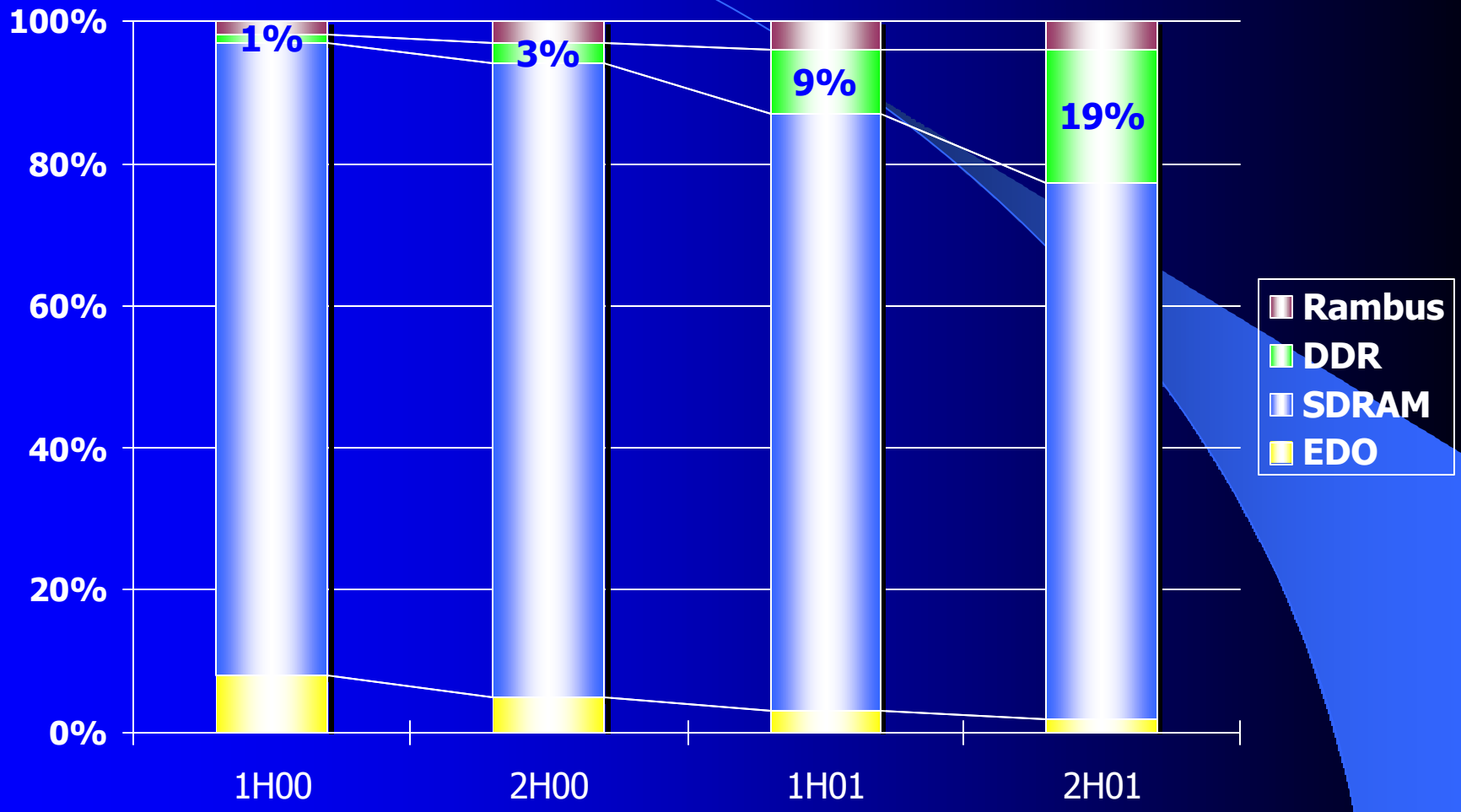
DRAM Market & Technology transition

DRAM Technology Transition



- Compiled from customer surveys
- Courtesy: Hyundai

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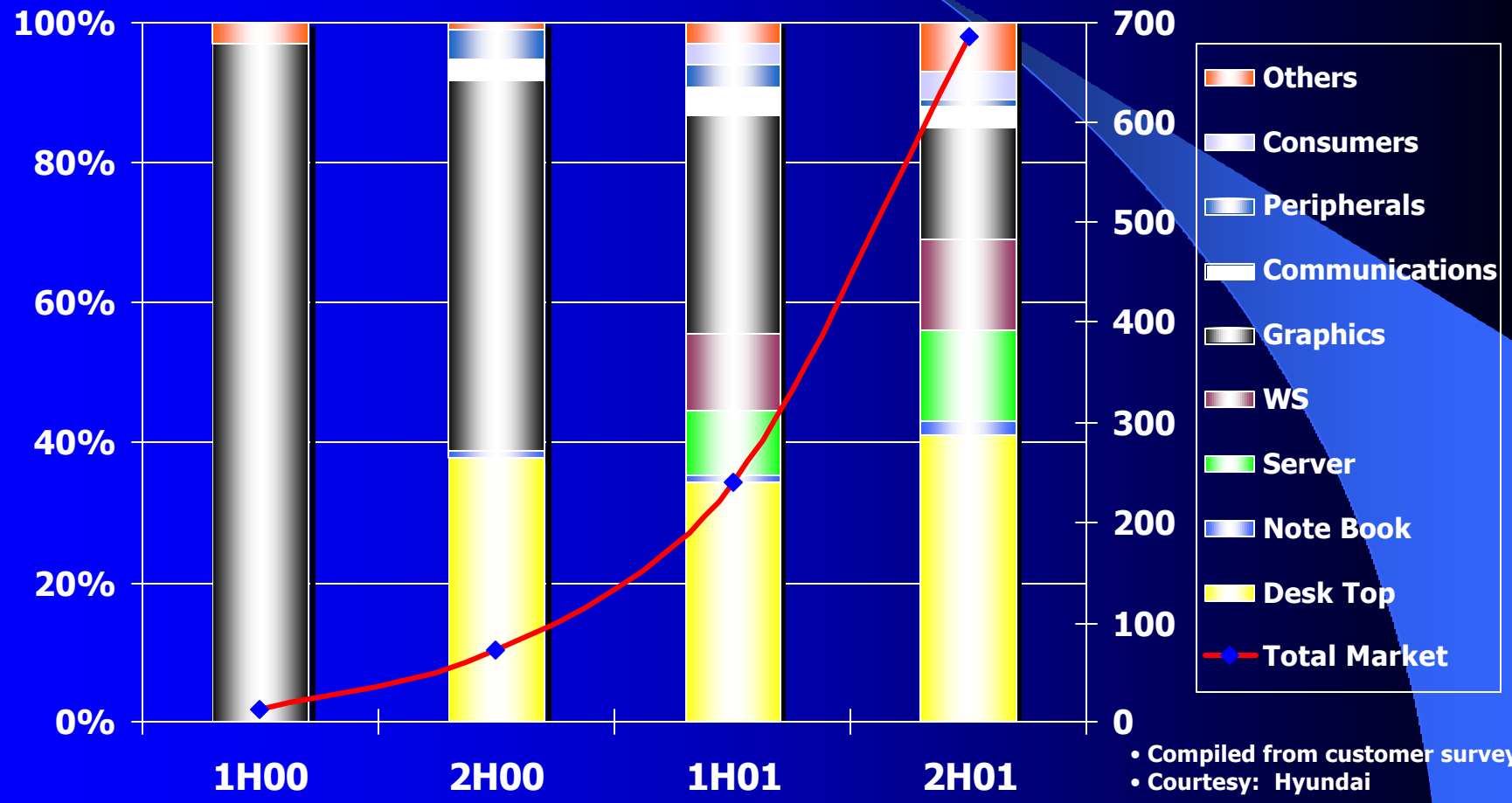
DDR Market Forecasts



- Compiled from customer surveys
- Courtesy: Hyundai

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Wide industry supply for DDR

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DDR Market in wide range of applications

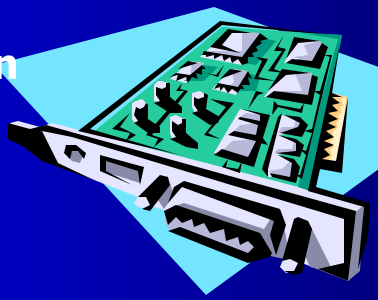
Reliability

Scalable I/O configuration support ECC and Chip Kill

Availability

Low cost manufacturing in terms of package, test and yields

Low power consumption 2.5V signaling



High bandwidth w/ source synchronized scheme

DDR Industry Status

Industry Update

- **DDR Device and DIMM support is ready**
  - Industry standard specification has been completed by JEDEC
  - Component Specification - DDR266A,B and DDR200
  - DIMM Specification and common gerber are completed for easy acceptance
    - 184P Unbuffered & Registered DIMM for Desktop and Server.
    - 200P SO-DIMM for Portable application.
- **DDR Platform is ready**
  - DDR platform have been fully simulated and physically validated
  - Major PC-OEM has started volume shipment
  - DDR support logic chips - PLL, Register and socket is available in market place
- **Industry Infrastructure is ready for DDR volume shipment**

DDR Platform Development Update

Chipset Company		1Q. 00	2Q. 00	3Q. 00	4Q. 00
A	Foster DDR200	H/W Validation			Production : 1Q. 01
B	Foster DDR200	Test Evaluation	H/W Validation		Production : 1Q. 01
C	Athlon PC200/266	H/W Validation		Production : 3Q. 00	
D	Athlon/P6 PC200/266	H/W Validation		Production : ?	
E	Athlon/P6 PC200/266	MB Simulation/Design		H/W Validation	Production : 10.00
F	Athlon/P6 PC200/266			H/W Validation	Production : 4Q.00
G	PC266	H/W Validation		Production : 3Q.00	

DDR Chipset and MB are now available in Market Place.
Bunch of DDR products launching is scheduled on 1Q01

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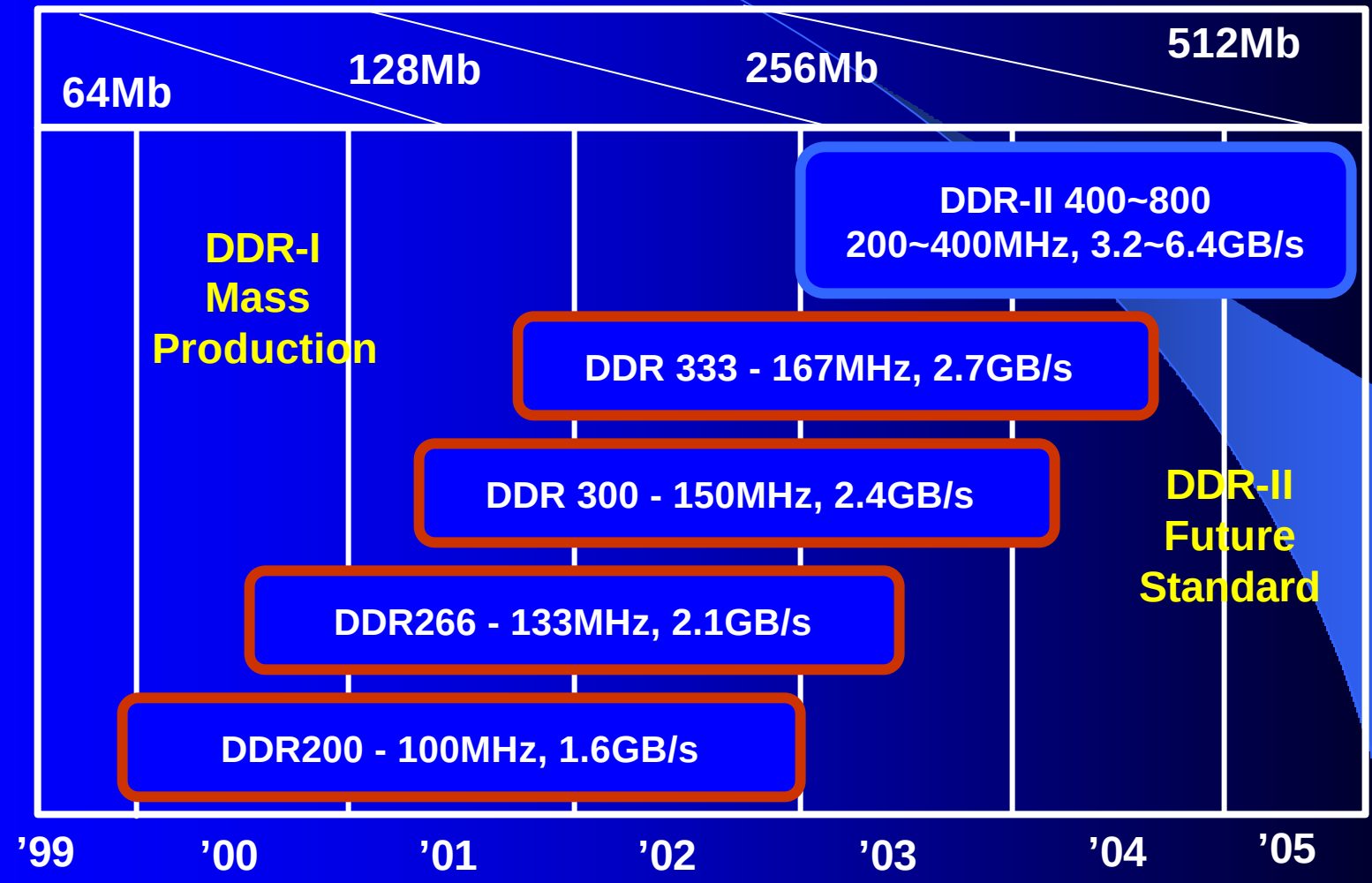
DDR DIMMs Develop. Status

-	R/C Rev.#	Data Width	Base. C	Banks	Memory Bus Routing	Dimensions
UB	R/C A1	x64/72	x8	1	60 ohm +/-10% two signal layers	1.25” height 5.25" length six-layer
	R/C B1	x64/72	x8	2/1		
	R/C C1	x64	x16	1		
RG	R/C A1	x64/72	x8	1	60 ohm +/-10% two signal layers	1.7” height 5.25" length eight-layer
	R/C B2	x72	x4	2/1		
	R/C C1	x72	x4	1		
SO	R/C A0	x64	x16	1,2	60 ohm +/-10% two signal layers	1.0" or 1.25" height 2.66" length six-layer
	R/C B0	x64	x8	1		
	R/C C0	x72	x16	1		

184P UB/RG, 200P SO DIMM Spec/Gerber completed.

DDR Performance Path Migration



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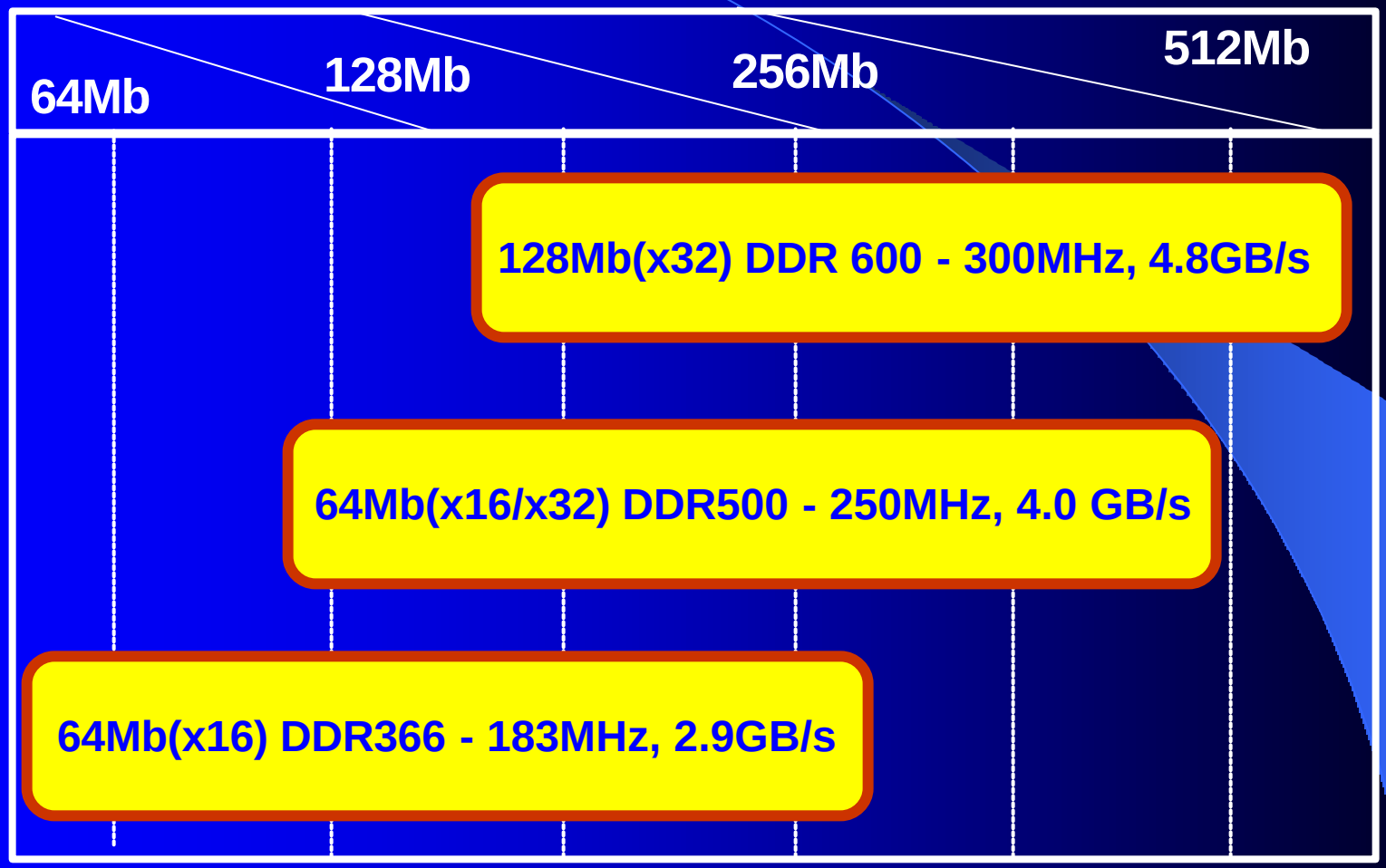
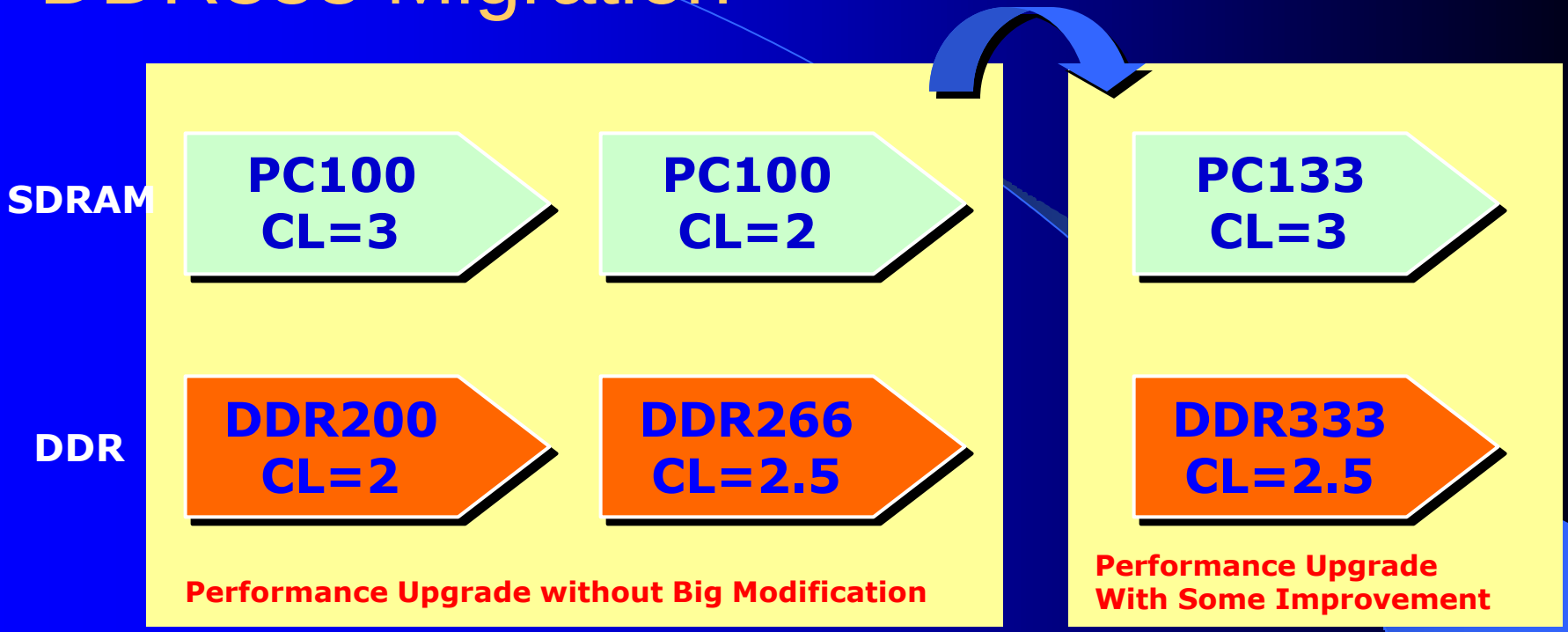
Point to Point DDR Performance



DDR333 Migration



- DDR333 is a Smooth Migration if we Recollect the History of SDRAM
- DDR333
  - Easily Accommodate 166MHz/333Mbps with ~0.13um Technology
  - With 2 Bit Prefetch, can Fill the Gap between DDR266 and DDR-II(400)
  - Fully Compatible with DDR200/266

DDR333 Branching with Package Type

DDR333 TSOP

- Same Parasitic RLC Requirements as DDR266
- Same Level of DLL Characteristics
  : Not Tightened tAC or tDQSCK
- 400ps tDS/tDH, 750ps tIS/tIH
- Fits for High Density, First Generation DDR

- Good for Small System & Low-end Desk-Top
- Possibly 2 Slots with 2 Banks with Un-buffered Module
- DRAM Supplier Can Have Some Headroom to be Prepared with High-Performance Design

DDR333 FBGA

- Tightened Parasitic RLC Requirements
- Same Level of DLL Characteristics
  : Not Tightened tAC or tDQSCK
- Timing : 350ps tDS/tDH, 600ps tIS/tIH
- Fits for High Density, Shruken Generation DDR
- Not to be in a Stream Path toward DDR-II

- Good for High-end System & Servers
- Multi- Slots with 2 Banks with Registered Module
- DRAM Supplier Can Have Some Headroom to be Prepared with DDR-II

- **Separate Foot-print of Module PCB for the Two Versions**
- **DRAM Supplier Must Forecast Pre-packaging Speed Bins**

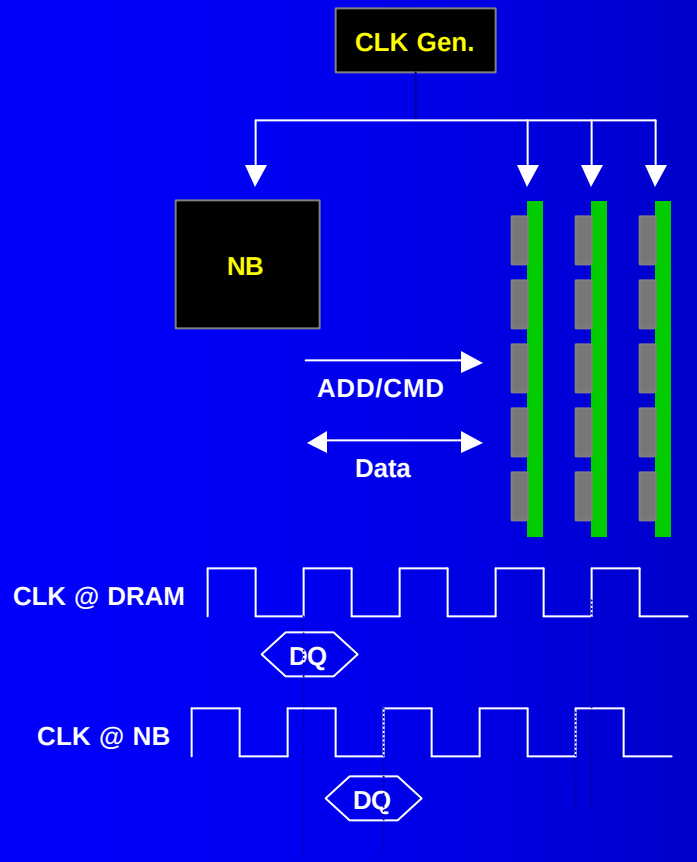
DDR Features, Performance Bench Marking

DDR SDRAM Features

- **Source Synchronous Clock Scheme**
  - **Address/command referenced to Clock as like PC100/133**
  - **Eliminates uncertainty between driver and receiver**
- **Terminated I/O Interface SSTL_2**
  - **Allow high speed interface with lower signal swing**
- **Differential Clock**
  - **Differential clock pair provide accurate clock to DRAM**
- **2.5 volt power supply**
  - **Low power consumption**

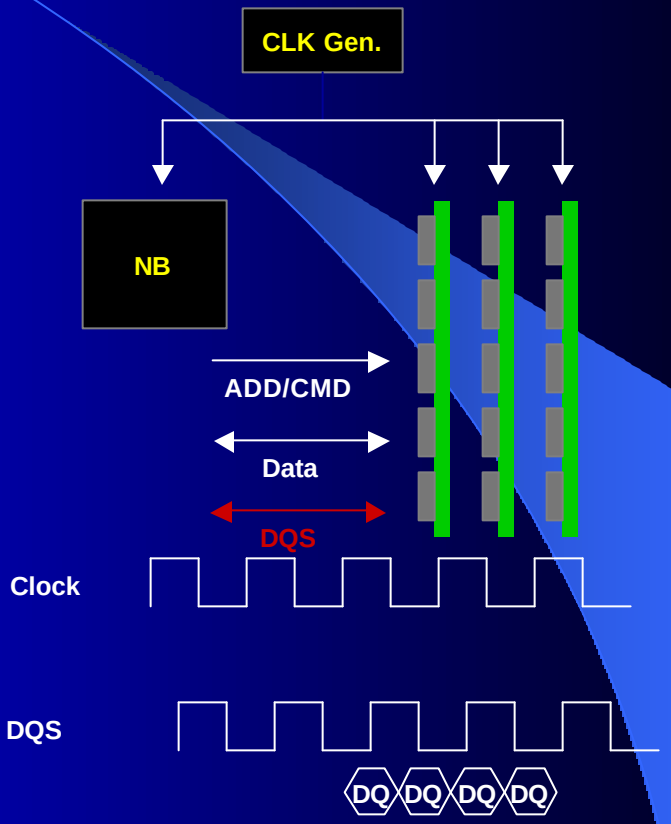
Source Synchronous Scheme

Clock Synchronous Scheme



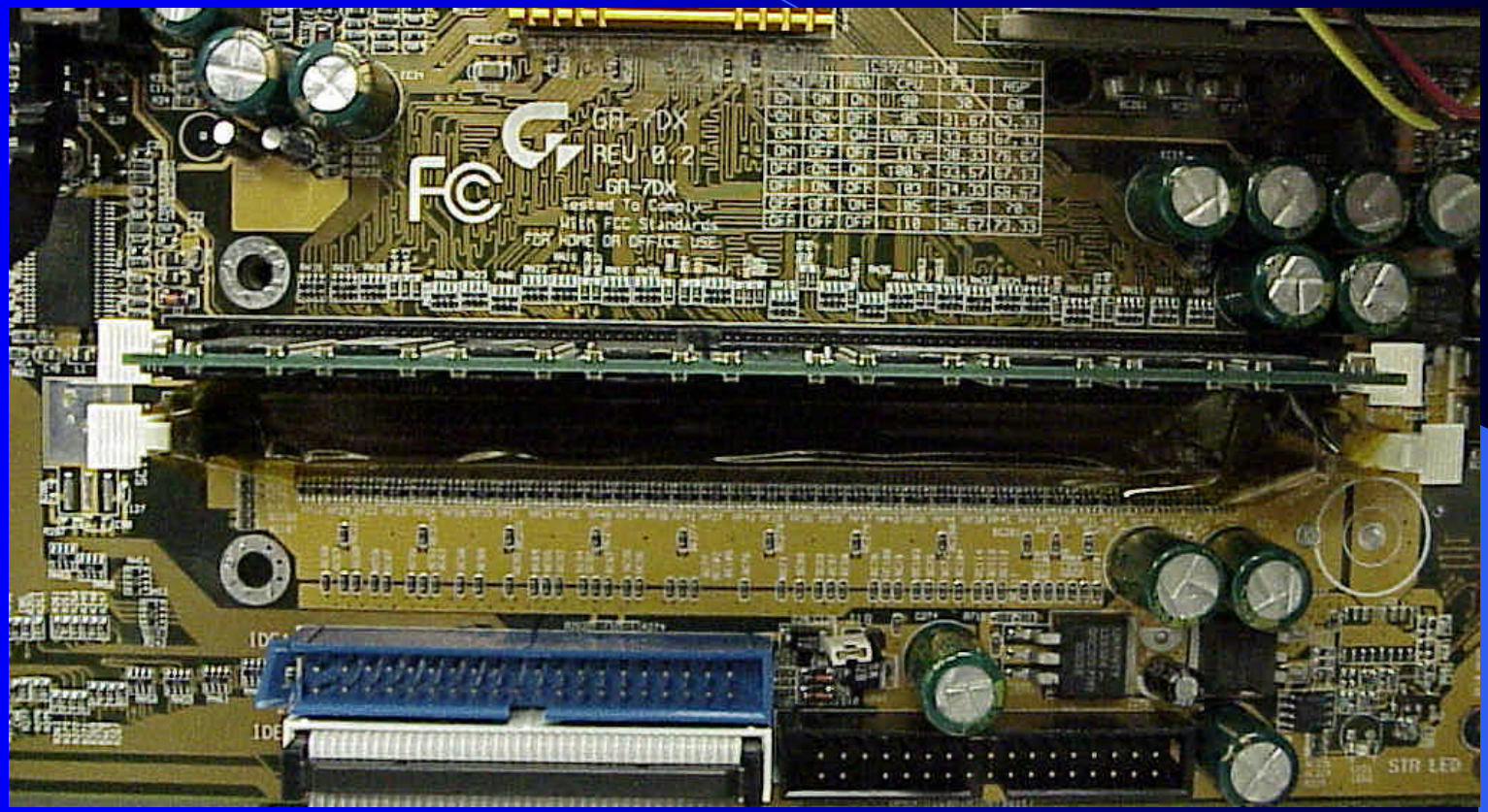
1 Clock Cycle > Flight Time + Valid Data + Clock Skew + Setup Time

Source Synchronous Scheme



Eliminates Uncertainty
Flight time, Clock Skew

DDR Platform - AMD



Gigabyte GA-7DX

DDR266 S/I Measurement

Unit : ns

Parameters	#1 RANK	#2 RANK	#3 RANK	#4 RANK
tIS - command	4.3	4.2	.4.1	4.1
tIH - command	2.2	2.1	2.1	2.1
tIS - Address	4.2	3.9	3.9	3.9
tIH - Address	1.9	2.1	2.2	2.2
tDS	1.58	1.60	1.52	1.52
tDH	1.16	1.54	1.16	1.30

Gigabyte PC266 Platform, AMD 761 Chipset, Unbuffered DIMM

Number of memory slots : 2 ea

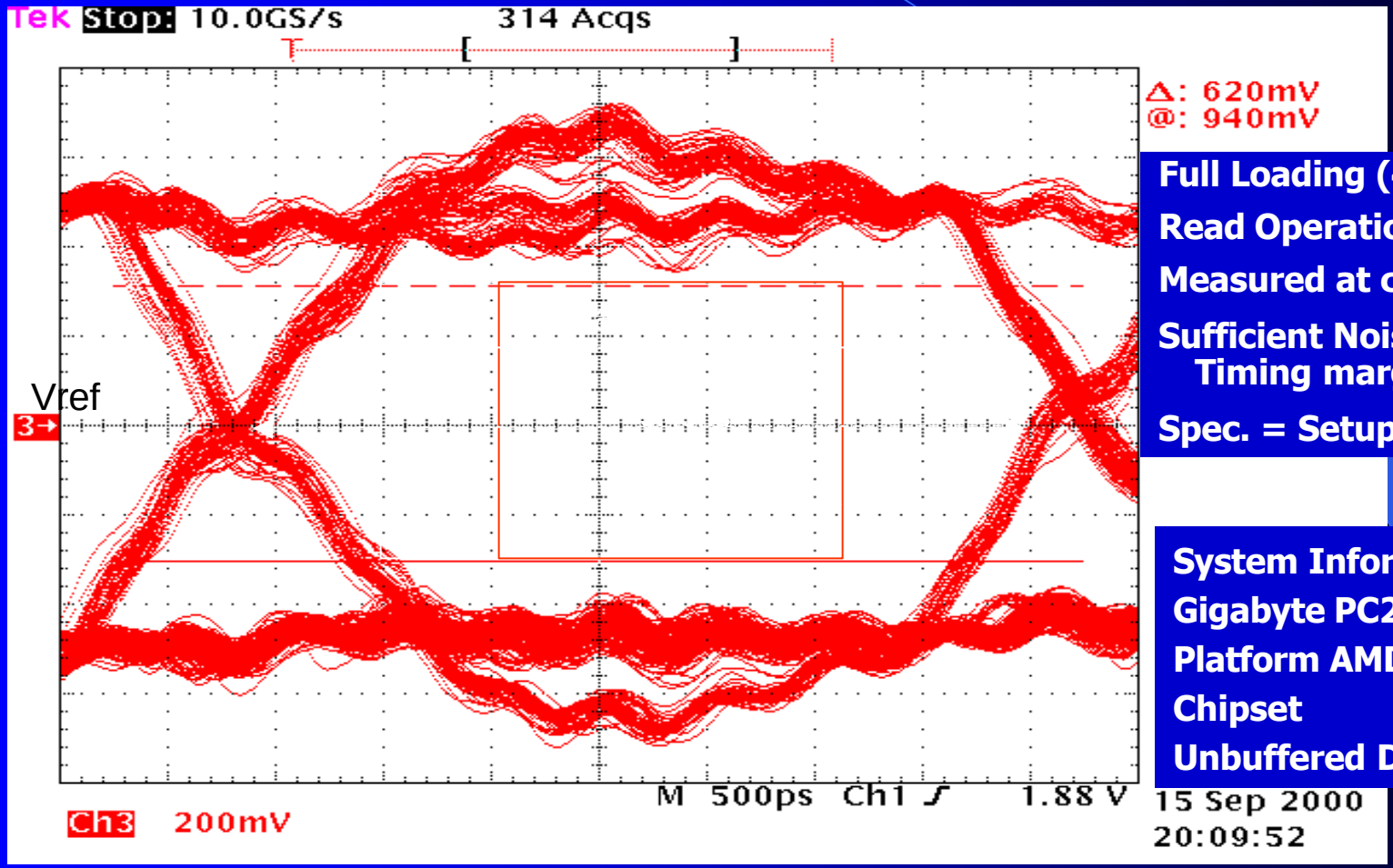
Number of memory banks : 4 banks

Maximum Load condition for Signals

- CS : 9 devices, Address/RAS/CAS/WE/CKE : 18 devices , DQ/DQS : 4 devices

DDR266 UB DIMM Read Data Eye

- Full loading, 4banks -



Full Loading (4 Rank)

Read Operation

Measured at chipset

Sufficient Noise and Timing margin

Spec. = Setup + Hold Time

System Information :

Gigabyte PC266

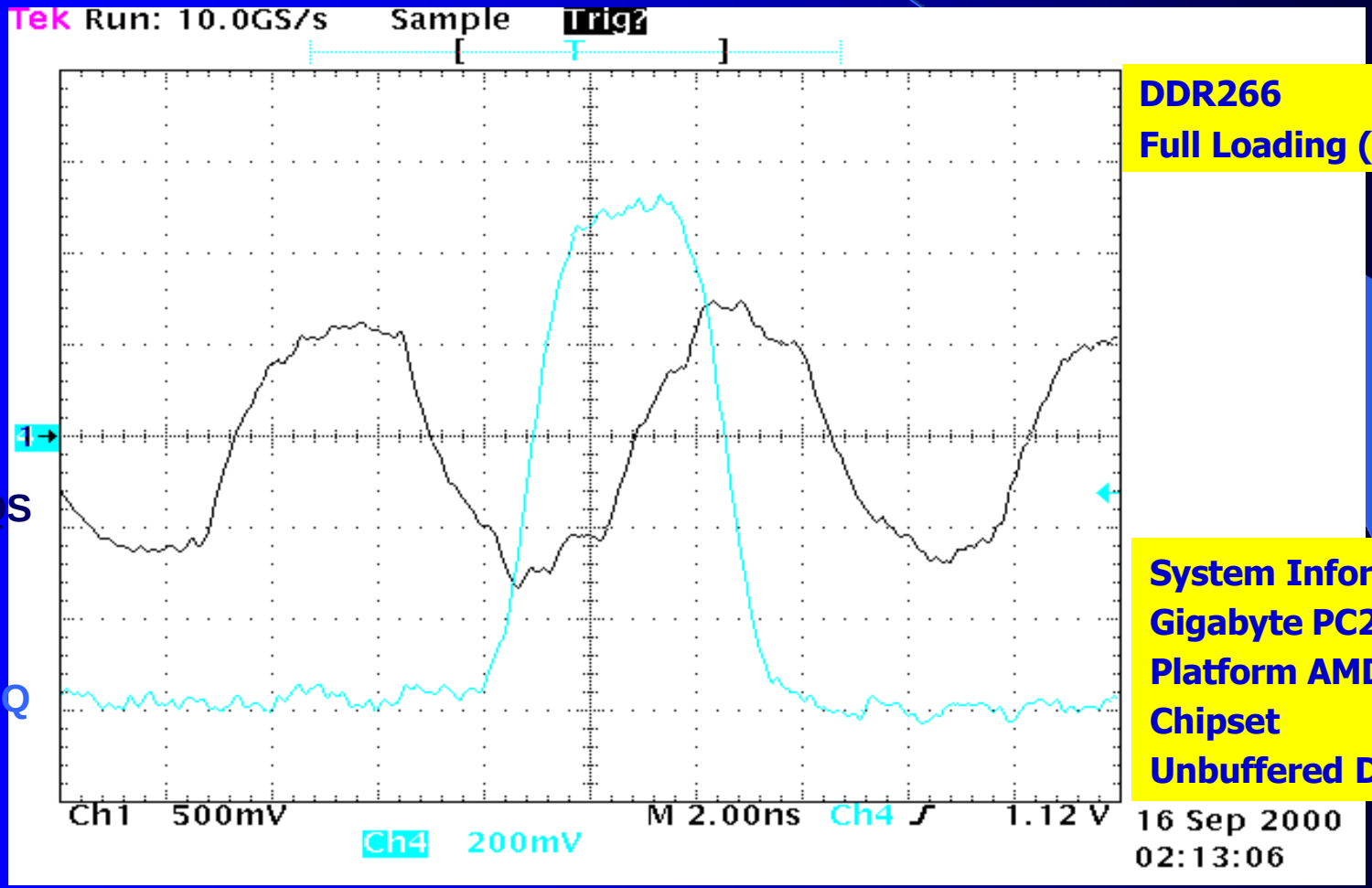
Platform AMD 761

Chipset

Unbuffered DIMM

DDR266 DQS/DQ Waveform

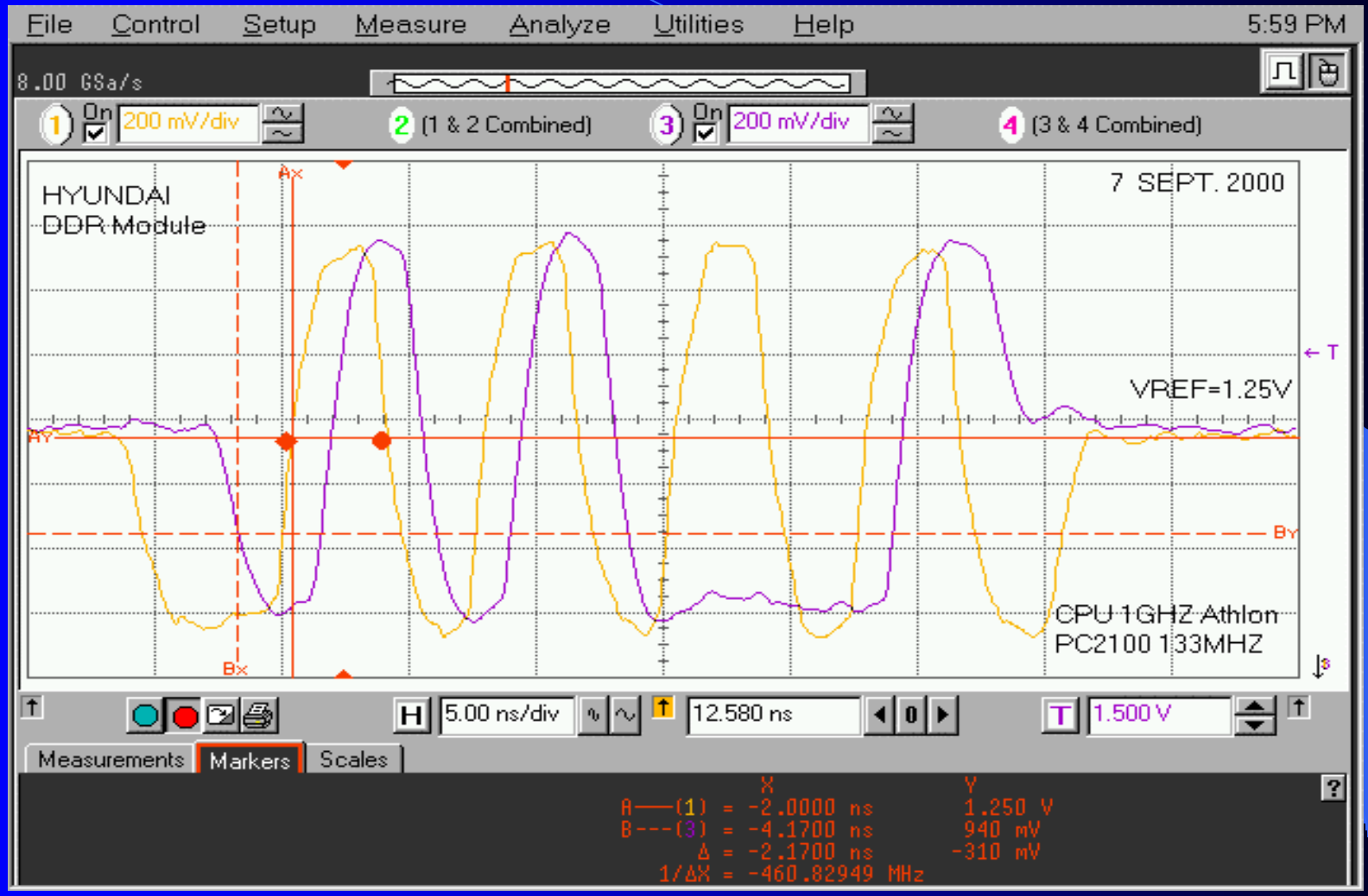
Write case, full loading, 4banks



DDR266
Full Loading (4 Rank)

System Information :
Gigabyte PC266
Platform AMD 761
Chipset
Unbuffered DIMM

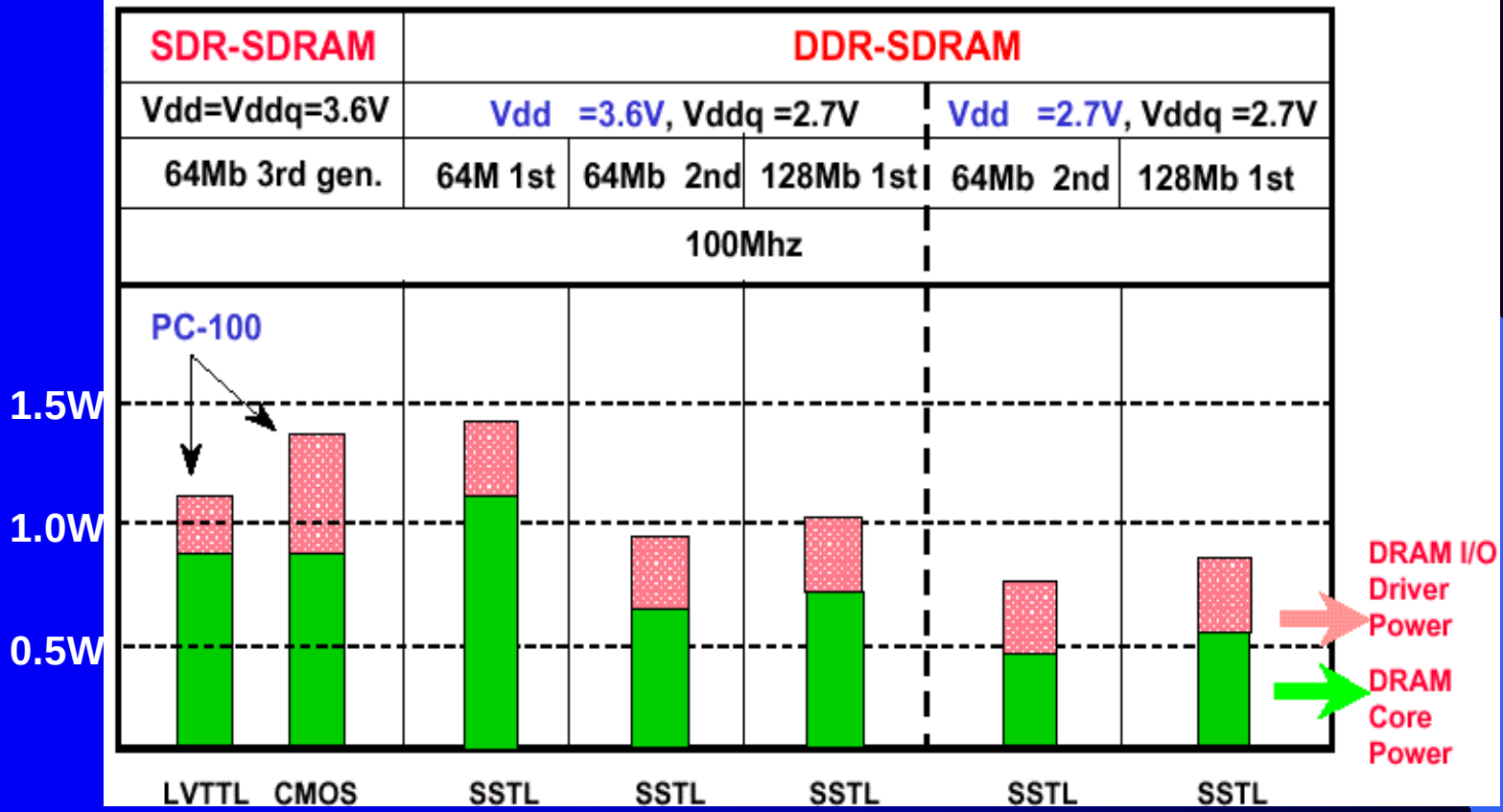
DDR266 Write Burst (Full loading)



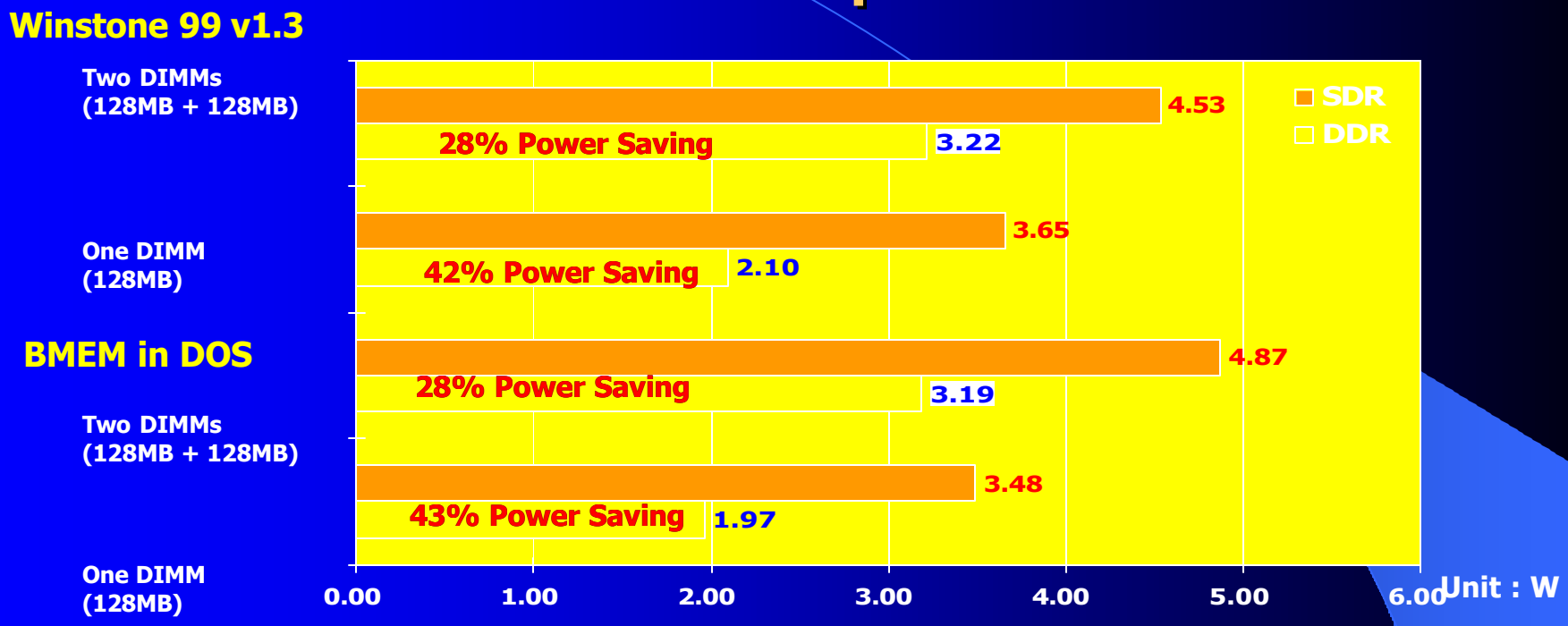
System Information : Gigabyte PC266 Platform, AMD 761 Chipset, Unbuffered DIMM,

Power Estimation of DDR SDRAM

- X16 org.
- Temp.=-5'C, 4Bank, Gapless Read Operation



Memory System Power Consumption



DDR Power Consumption include ;
- North Bridge Core Power
- Memory I/O & DIMM
- Clock Generator
- Voltage Regulator & VTT termination

SDR Power Consumption include ;
- North Bridge Core Power
- Memory I/O & DIMM
- Clock Generator

Source : ALi

Benchmarking System Information

Platform Configuration

	CPU	FSB	CHIP-SET	MAIN MEMORY	MEM. CLOCK	GRAPHIC CARD	OS	HDD
GIGABYTE GA-7DX REV1.1 DDR	AMD ATHLON 800MHZ 256KB	200MHZ	AMD 761	HYMD1166458-H DDR SDRAM 128MB	100MHZ CL2	AGP 4X MATROX MILLENIUM G400	WIN98	FUJITSU MPE3043AE UDMA 66
MICRO STAR K7T PRO VER.1 SYNC.	AMD ATHLON 800MHZ 256KB	200MHZ	VIA KT133	HYM71V651601TH-10P SDRAM PC100 128MB	100MHZ CL2	AGP 4X MATROX MILLENIUM G400	WIN98	FUJITSU MPE3043AE UDMA 66
INTEL SOLANO SYNC	PIII 800MHZ 256KB	133MHZ	I815	HYM71V631601TH-75 SDRAM PC133 128MB	133MHZ CL3	AGP 4X MATROX MILLENIUM G400	WIN98	FUJITSU MPE3043AE UDMA 66

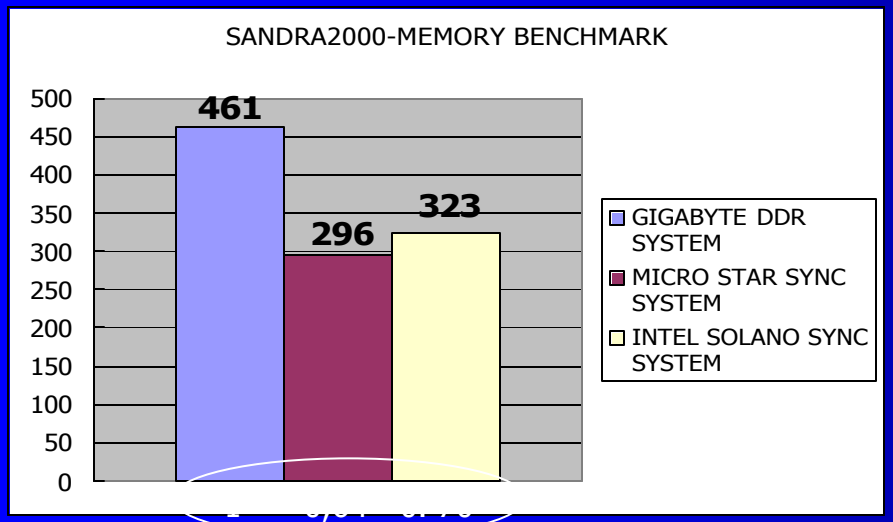
Memory Module Configuration

AC PARAMETER	tRCD	tRRD	tRC	tRP	tRAS
***DDR SDRAM**	Min 20nsec	Min 15nsec	Min 65nsec	Min 20nsec	Min 48nsec
****SDRAM**	Min 20nsec	Min 15nsec	Min 65nsec	Min 20nsec	Min 45nsec

Memory Sub-system Benchmark

SANDRA2000 Performance

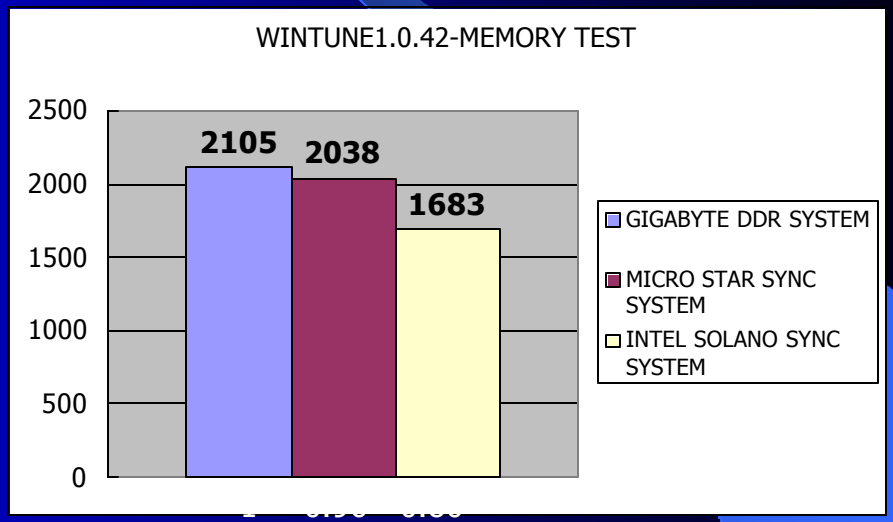
TEST ITEM: MEMORY BENCHMARK



Normalized to DDR

WINTUNE1.0.42 Performance

TEST ITEM: MEMORY TEST



This result shows memory subsystem(memory, CPU, chip-set, cache) performance comparison in windows system.

Sandra2000 Data shows CPU/Memory Bandwidth(MB/S).

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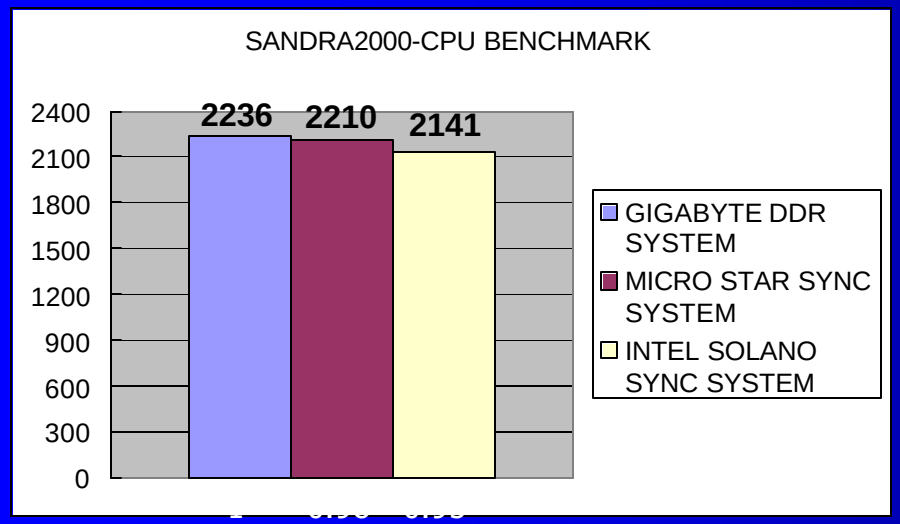
System Productivity Benchmark

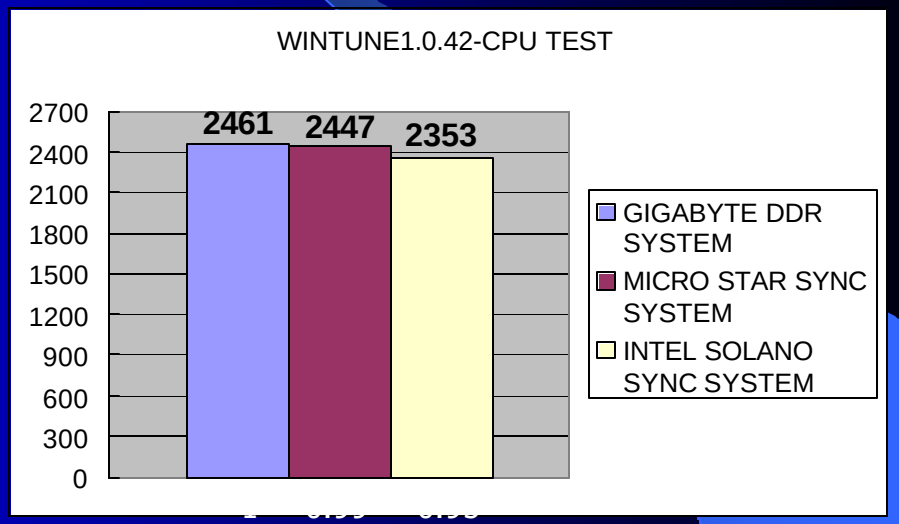
SANDRA2000 Performance

TEST ITEM: CPU BENCHMARK



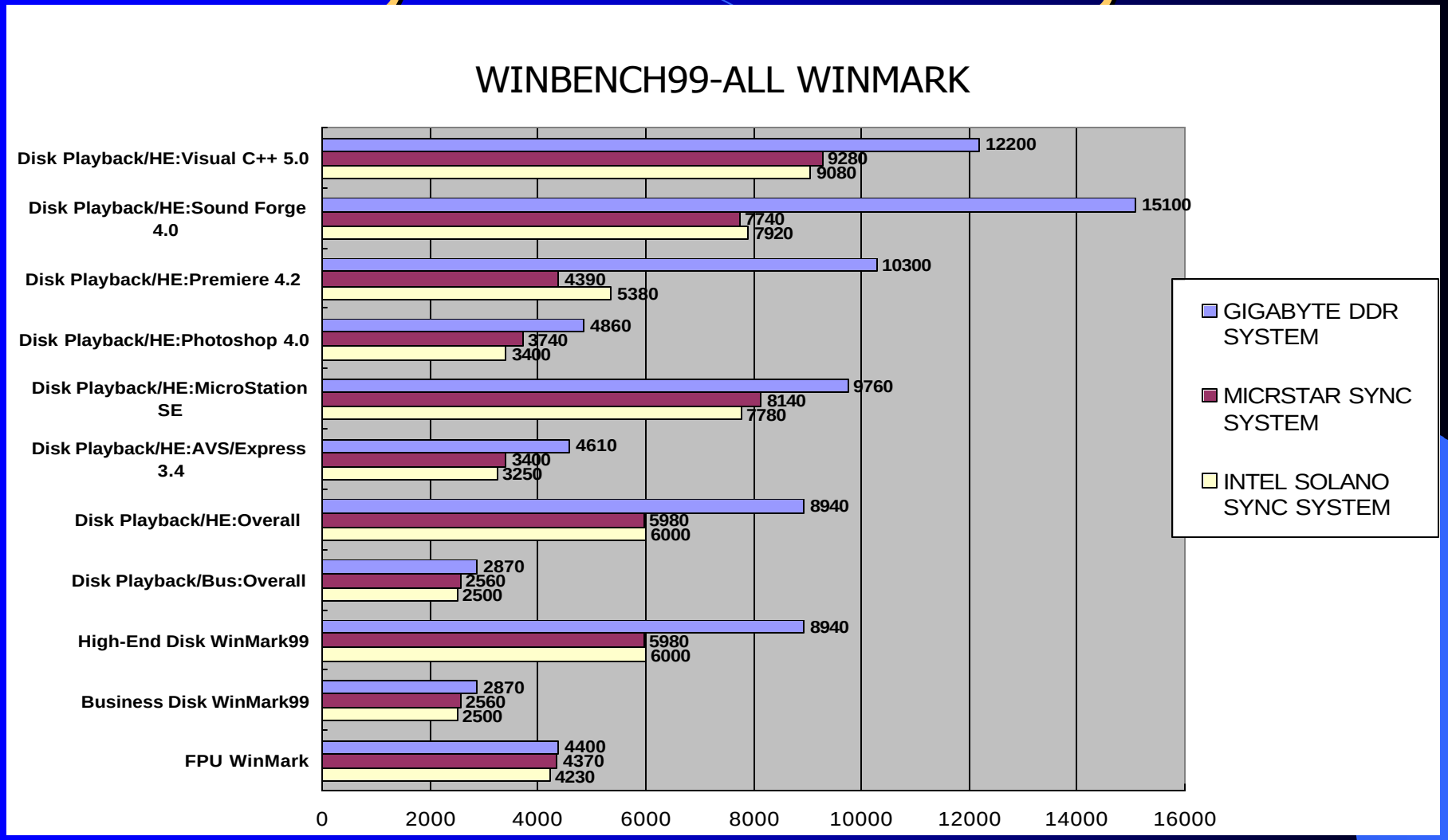
WINTUNE1.0.42 Performance

TEST ITEM: CPU TEST



This shows how CPU and internal cache system stack up to other typical combination in a windows system.

System Productivity



Hyundai DDR SDRAM

Hyundai DDR SDRAM Update

- **64/128/256M DDR Components**
  - 64/128Mb DDR PC200/PC266B in production
  - 256Mb DDR volume production will start from 4Q00
- **DDR DIMM Modules**
  - Continue to enable and support industry common gerber
  - Continue to work closely with industry partners such as Chipsets, PC OEMs, and infrastructure companies
  - All Unbuffered & Registered DIMM are available now
- **High Speed - wide I/O DDR Components for point to point applications**
  - 2Mx32 DDR 166/183Mhz available and production is ramping up
  - Multiple options/features for high speed interface operation
  - Developing next generation 300MHz 2/4Mx32 DDR

Hyundai DDR DRAM Family

4th 64M DDR — MP
PC-266A, SS-333

2Mx32 DDR — ES
SS-333

2nd 128M DDR — MP
PC-266B

5th 64M DDR — P
PC-266A, PC-333, SS-466

3rd 128M DDR — ES
PC-266A, PC-333/400

4Mx32 DDR — D
SS-400 ~ 600

2Mx32 DDR — D
SS400 ~600

- All generations except 4th 64M (including x32) are equipped with QFC switch
- All generations except 4th 64M DDR (not x32) are equipped with Half Strength Driver
- All support CL = 2, 2.5, 3

2nd 256M DDR — P
PC-266A, PC-300, SS-333

3rd 256M DDR — D
PC-266A, PC-333, SS-400

1st 512M DDR — D
PC-266A

D — Design
P — Wafer Processing
ES — Functionality Proven
MP — Mass Production

A -Tech *B -Tech* *C -Tech* *D -Tech*

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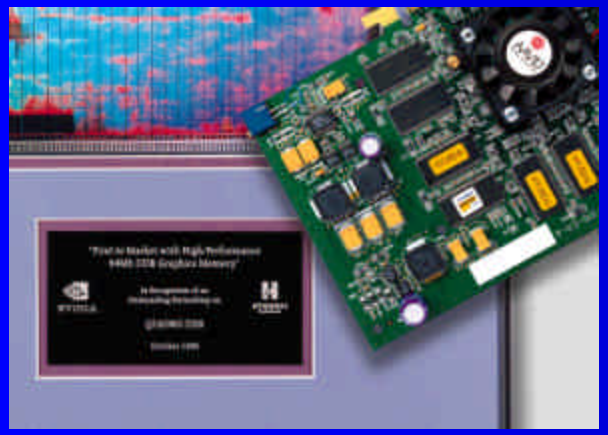
Hyundai DDR Strategy

1999

DDR Graphics Adoption



- World's first company to launch DDR technology in industry
- Support high speed 64Mb DDR in the volume production
  - 4Mx16 for High-end
  - 2Mx32 for Low-end

2000

Main Memory Enabling

- HE UNIX Server, WS
- NT PC Server, WS
- Desktop PC
- Portable PC

- JEDEC TG have defined common gerber for DDR market adoption.
- Major focus on validation and enabling activities
- Volume production will start from 2H00

2001 & Beyond

Volume Ramp-up & Expansion of other Application

- Consumer
- Networking
- Others

- Wide range of product family for emerging new applications
  - 512Mb for HE main memory application
  - Up to 300MHz for point to point application

Platform 2001

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Call to Action

- **Industry Partnership**
  - We believe industry partnerships are the most important activity to enable new technology
- **Hyundai is committed to have full resource to support this partnership**
- **Hyundai is actively promoting DDR with our partners**